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FACSIMILE TRANSMITTAL SHEET
DECEMBER 5, 2006

TO: Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RE: U.S. Patent Application No. **10/770,413**
For: METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES
Filing Date: 02/04/2004
Atty. Docket No. **1374.39158CX1**

From: Leonid D. Thenor

Fax Number: (571) 273-2885

Total Number of Pages: 5

Items Attached: Issue Fee Transmittal Form – 1 Page
Comments on Statement of Reasons for Allowance – 2 Pages
Credit Card Payment Form -- 1 Page

I hereby certify that on DECEMBER 5, 2006, the above-identified documents are being facsimile transmitted to the United States Patent and Trademark Office.

Ricardo E. Perez — Ricardo Perez
Name (Print) Signature

501.39158CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Hasegawa et al.
Serial No.:	10/770,413
Filed:	February 4, 2004
Title:	METHOD OF MAUFCATURING SEMICONDCUTOR INTEGRATED CIRCUIT DEVICES
Group:	1756
Examiner:	CHACKO DAVIS, Daborah
Confirmation No.:	1925

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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December 5, 2006

Sir:

Applicants note that in the Reasons for Allowance at page 2 of the Notice of Allowability dated September 5, 2006, the Examiner sets forth that "claims 1-18, are allowable over the prior art of record (U.S. Patent No. 6,327,022 (Nishi), U.S. Patent No. 6,544,721 (Saito), and U.S. Patent No. 6,103,428 (Hatai et al.)) because the prior art of record does not disclose the method of forming a semiconductor device wherein the phase of the light passing through all of the hole patterns of the first layout pattern is inverted from a phase of the light passing through all the hole patterns of the second layout pattern corresponding to the hole pattern of the first layout pattern."

In citing the art of record, Applicants note that the Examiner has omitted Japanese Patent No. JP 06-83032. This reference was included in the IDS filed with the application, and initialed by the Examiner on the Office Action dated March 28,

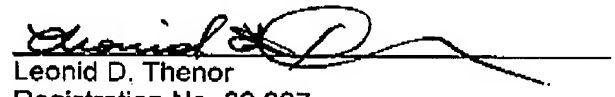
2005. In view of this reference, Applicants believe that the Reasons for Allowance should include this reference as follows:

> "claims 1-18, are allowable over the prior art of record (JP 06-83032, U.S. Patent No. 6,327,022 (Nishi), U.S. Patent No. 6,544,721 (Saito), and U.S. Patent No. 6,103,428 (Hatai et al.)) because the prior art of record does not disclose the method of forming a semiconductor device wherein the phase of the light passing through all of the hole patterns of the first layout pattern is inverted from a phase of the light passing through all the hole patterns of the second layout pattern corresponding to the hole pattern of the first layout pattern."

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 501.39158CX1).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP.



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Dated: December 5, 2006